DATA SHEET

SA8016

2.5GHz low voltage fractional-N synthesizer

Objective specification
Supersedes data of 1998 Apr 06

1998 Oct 13

Philips
Semiconductors

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2.5GHz low voltage fractional-N synthesizer SA8016

FEATURES

- Low phase noise
- Low power
- Fully programmable main divider
- Internal fractional spurious compensation
- Hardware and software power down

APPLICATIONS

- 800–2500 MHz wireless equipment
- PCS
- Cellular phones
- WLAN
- Portable battery-powered radio equipment.

General description

The SA8016 BICMOS device integrates programmable dividers, charge pumps and a phase comparator to implement a phase-locked loop. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 3 V supplies.

The synthesizer operates at VCO input frequencies up to 2.5 GHz. The synthesizer has fully programmable main and reference dividers. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DDCP} could be greater than or equal to V_{DD}.

The charge pump current (gain) is fixed by an external resistance at pin RSET (pin 10). Only passive loop filters are used; the charge-pump operates within a wide voltage compliance range to provide a wider tuning range.

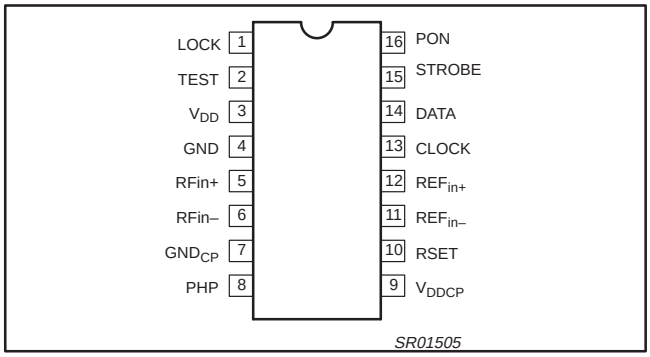


Figure 1. Pin Configuration

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage	V_{DD}	2.7	–	5.5	V
V_{DDCP}	Analog supply voltage	$V_{DDCP} \geq V_{DD}$	2.7	–	5.5	V
$I_{DDCP}+I_{DD}$	Supply current		–	8.0	9.5	mA
$I_{DDCP}+I_{DD}$	Total supply current in power-down mode		–	1	–	µA
f_{VCO}	Input frequency		800	–	2500	MHz
f_{REF}	Crystal reference input frequency		10	–	40	MHz
f_{PC}	Maximum phase comparator frequency		–		4	MHz
T_{amb}	Operating ambient temperature		–40	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SA8016	TSSOP16	Plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403–1

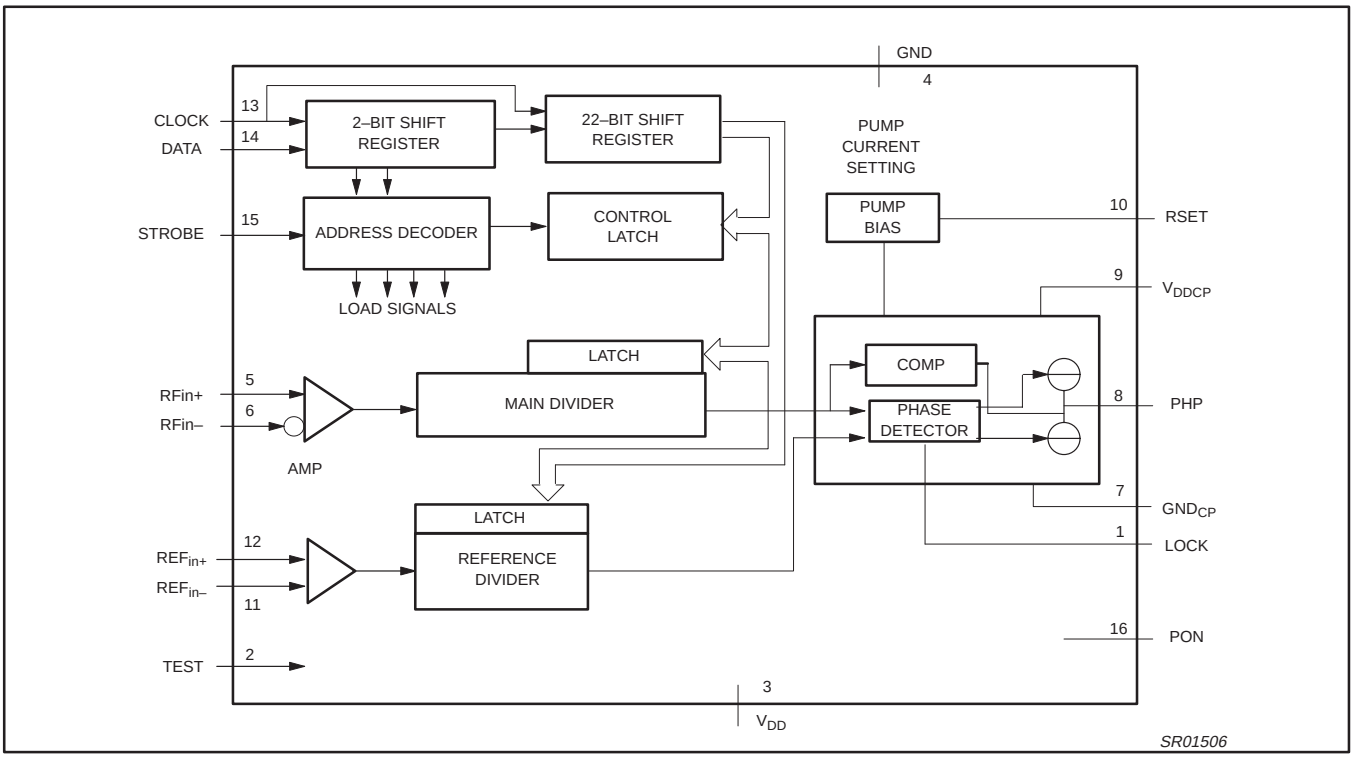


Figure 2. Block Diagram

PINNING

SYMBOL	PIN	DESCRIPTION
LOCK	1	Lock detect output
TEST	2	Test
V_{DD}	3	Digital supply
GND	4	Digital ground
RFin+	5	RF positive input to main divider
RFin–	6	RF negative input to main divider
GND_{CP}	7	Charge pump ground
PHP	8	Main NORMAL chargepump
V_{DDCP}	9	Charge pump supply voltage
RSET	10	External resistor from this pin to ground sets the chargepump current
$REF_{in–}$	11	Reference input
REF_{in+}	12	Reference input
CLOCK	13	Programming bus clock input
DATA	14	Programming bus data input
STROBE	15	Programming bus enable input
PON	16	Power down control

Characteristics

V_{DDCP} = V_{DD} = +3.0V, T_{amb} = +25°C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 3, 9						
V_{DD}	Digital supply voltage		2.7	–	5.5	V
V_{DDCP}	Analog supply voltage	V_{DDCP} = V_{DD}	2.7	–	5.5	V
$I_{DDTotal}$	Synthesizer operational digital supply current	V_{DD} = +3.0 V	–	8.0	9.5	mA
$I_{standby}$	Total supply current in power-down mode	logic levels 0 or V_{DD}	–	1	TBD	µA
RFin main divider input; pins 5, 6						
f_{VCO}	VCO input frequency		800	–	2500	MHz
$V_{RFin(rms)}$	AC-coupled input signal level	R_s = 50 Ω; MAX. limit is indicative	–18	–	0	dBm
Z_{IRFin}	Input impedance (real part)	f_{VCO} = 2.0 GHz	–	TBD	–	kΩ
C_{IRFin}	Typical pin input capacitance	indicative, not tested	–	TBD	–	pF
N_m	Main divider ratio		512	–	65535	
f_{PCmax}	Maximum loop comparison frequency	indicative, not tested	–	–	4	MHz
Reference divider input; pins 11, 12						
f_{REFin}	Input frequency range from crystal		10	–	40	MHz
VRFin	AC-coupled input signal level	R_S=50Ω; MAX. limit is indicative	360	–	1300	mVpp
Z_{REFin}	Input impedance (real part)		–	TBD	–	kΩ
C_{REFin}	Typical pin input capacitance	indicative, not tested	–	TBD	–	pF
R_{REF}	Reference division ratio		4	–	1023	
Charge pump current setting resistor input; pin 10						
R_{SET}	External resistor from pin 3 to ground		6	7.5	24	kΩ
V_{SET}	Regulated voltage at pin 3	R_{SET}=7.5 kΩ	–	1.25	–	V
Charge pump outputs (including fractional compensation pump); pins 8; R_{SET} =7.5 kΩ, FC=80						
Icp	Charge pump current ratio to Iset	Current gain I_{PH}/I_{SET}	–15		+15	%
I_{MATCH}	Sink-to-source current matching	V_{ph}=1/2 V_{DDCP}.	–10		+10	%
I_{ZOUT}	Output current variation versus Vph[2]	V_{ph} in compliance range	–10		+10	%
I_{LPH}	Charge pump off leakage current	V_{cp}=1/2 V_{CC}	–10		+10	nA
V_{ph}	Charge pump voltage compliance		0.7	–	V_{DDCP}–0.8	V
Phase noise						
C/N	Synthesizer's contribution to close-in-phase noise of 2100 MHz RF signal at 1 kHz offset.	fref=19.44MHz; fcomp=240kHz indicative, not tested	–	–75	–	dBc Hz
Interface logic input signal levels; pins 3, 11, 12, 14, 15, 16						
V_{IH}	HIGH level input voltage		0.7*V_{DD}	–	V_{DD}+0.3	V
V_{IL}	LOW level input voltage		–0.3	–	0.3*V_{DD}	V
I_{bias}	Input bias current	logic 1 or logic 0	–5	–	+5	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Lock detect output signal (in push/pull mode); pin 1						
V_{OL}	LOW level output voltage	I_{sink} = 2mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{source} = –2mA	V_{DD}–0.4	–	–	V

NOTES:

1. $I_{SET} = \frac{V_{SET}}{R_{SET}}$ bias current for charge pumps.

2. The relative output current variation is defined thus:

$$\frac{\Delta I_{OUT}}{I_{OUT}} = 2 \cdot \frac{(I_2 - I_1)}{|(I_2 + I_1)|}; \text{ with } V_1 = 0.7V,\ V_2 = V_{DDCP} - 0.8V \text{ (See Figure 3.)}$$

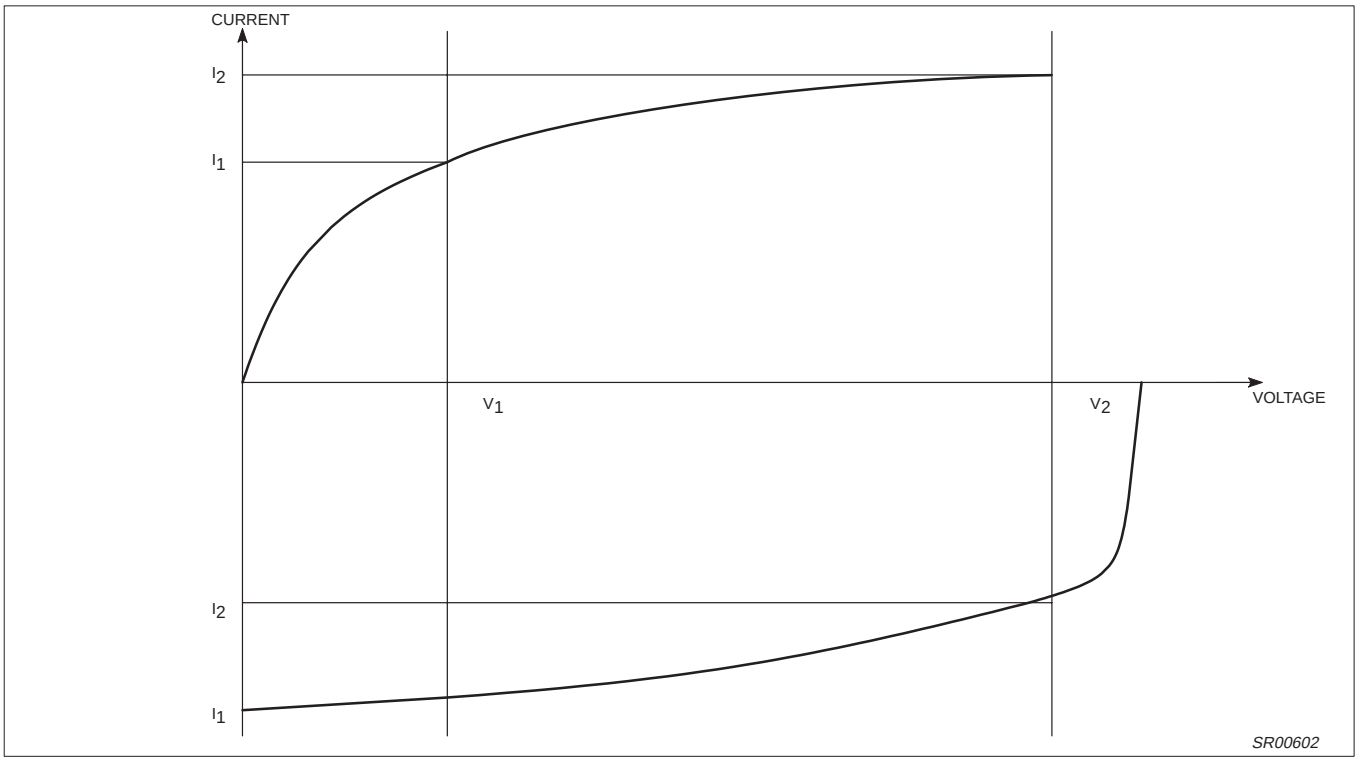


Figure 3. Relative Output Current Variation

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Digital supply voltage	–0.3	+5.5	V
V_{DDCP}	Analog supply voltage	–0.3	+5.5	V
$\Delta V_{DDCP}–V_{DD}$	Difference in voltage between V_{DDCP} and V_{DD} ($V_{DDCP} \geq V_{DD}$)	–0.3	+2.8	V
V_n	Voltage at pins 1, 2, 5, 6, 11 to 16	–0.3	V_{DD} + 0.3	V
V_1	Voltage at pin 8, 9	–0.3	V_{DDCP} + 0.3	V
ΔV_{GND}	Difference in voltage between GND_{CP} and GND (these pins should be connected together)	–0.3	+0.3	V
P_{tot}	Total power dissipation		TBD	mW
T_{stg}	Storage temperature	–55	+125	°C
T_{amb}	Operating ambient temperature	–30	+85	°C
T_j	Maximum junction temperature		TBD	°C

Handling

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j–a}$	Thermal resistance from junction to ambient in free air	120	K/W

FUNCTIONAL DESCRIPTION

Main Fractional-N divider

The RFin input (pins 5 and 6) drive a pre-amplifier to provide the clock to the first divider stage. For single ended operation, the signal should be fed to one of the inputs while the other one is AC grounded. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from –18dBm to +0dBm, and at frequencies as high as 2.5 GHz. The divider consists of a fully programmable bipolar prescaler followed by a CMOS counter. Divide ratios (512 to 65536) allow a minimum phase comparison frequency of 25kHz at 2.5 GHz RF.

At the completion of a main divider cycle, a main divider output pulse is generated which will drive the main phase comparator. Also, the fractional accumulator is incremented by the value of NF. The accumulator works with modulo Q set by FMOD. When the accumulator overflows the overall division ratio N will be increased by 1 to N + 1, the average division ratio over Q main divider cycles (either 5 or 8) will be

$$Nfrac = N + \frac{NF}{Q}$$

The output of the main divider will be modulated with a fractional phase ripple. The phase ripple is proportional to the contents of the fractional accumulator and is nulled by the fractional compensation charge pump.

The reloading of a new programming word is synchronized to the state of the main divider to avoid introducing a phase disturbance.

Reference divider

The reference divider consists of a divider with programmable values between 4 and 1023 followed by a three bit binary counter. The 3 bit SM (SA) register (see figure 4) determines which fo the 5 output pulses are selected as the main (auxiliary) phase detector input.

Phase detector

The reference and main (aux) divider outputs are connected to a phase/frequency detector that controls the charge pump. The pump current is set by a an external resistor. The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by forcing the pumps ON for a minimum time at every cycle (backlash time) providing improved linearity.

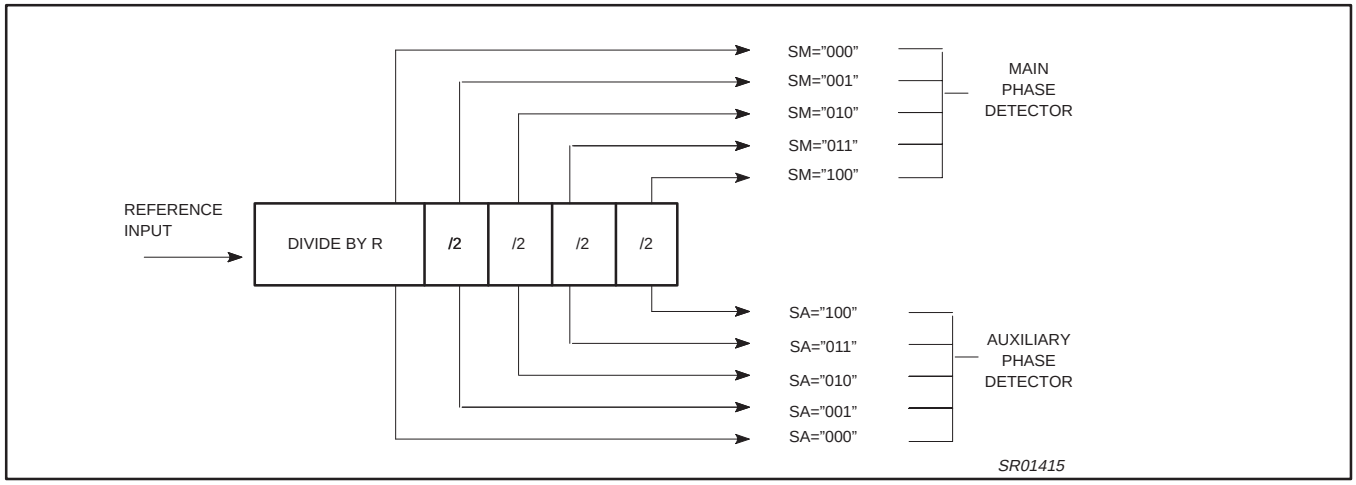


Figure 4. Reference Divider

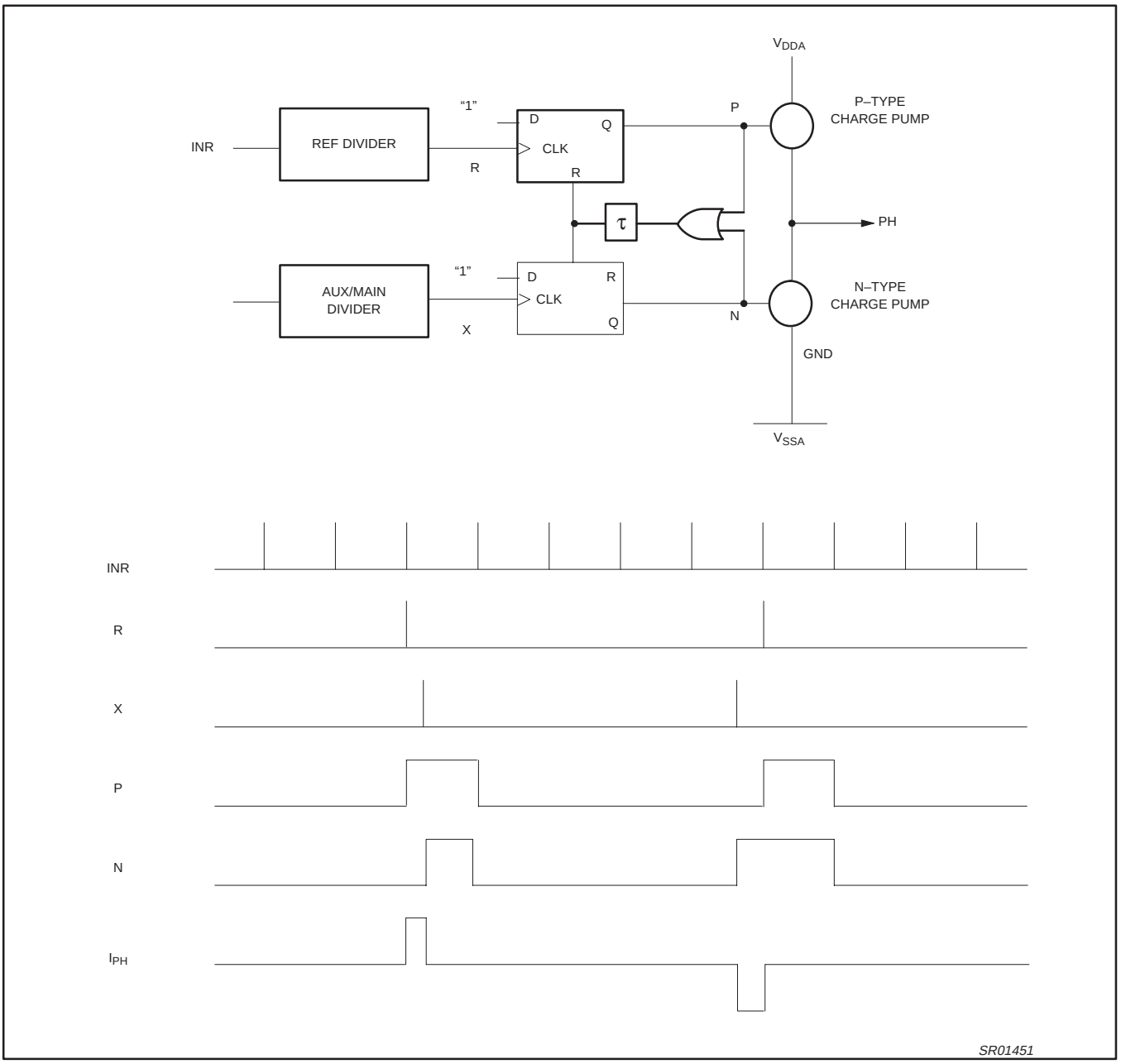


Figure 5. Phase Detector Struction with Timing

Main Output Charge Pumps and Fractional Compensation Currents.

The main charge pumps on pins PHP and PHI are driven by the main phase detector and the charge pump current values are determined by the current at pin RSET. The fractional compensation is derived from the current at RSET, the contents of the fractional accumulator FRD and by the program value of the FDAC. The timing for the fractional compensation is derived from the main divider. See table of charge pump ratios.

Principle of Fractional Compensation

The fractional compensation is designed into the circuit as a means of reducing or eliminating fractional spurs that predominate when the accumulator rolls over and the main divider counts one extra RF input cycle (+1, swallows a cycle). Since I_{COMP} is the compensation current and I_{PUMP} is the pump current, for each charge pump,

$$I_{PUMP\_TOTAL} = I_{PUMP} + I_{COMP}.$$

The theoretical values for FDAC are: 128 for FMOD = 1 (modulo 5) and 80 for FMOD = 0 (modulo 8). Fractional division will cause the pump to output a charge that is compensated for in order to reduce fractional spurs. This compensation is done by sourcing a small current, i_A, see Figure 7, that is proportional to the fractional error phase. Figure 6 shows that for proper fractional compensation, the area of the fractional compensation current pulse must be equal to the area of the charge pump ripple.

This means $I_{PUMP}*Q=I_{COMP}*128$, where Q equals fractional-N modulus e.g., 2/5 for NF = 2 and FMOD = 1. The fractional compensation current is derived from the main charge pump in that it follows all the current scaling through external resistor setting, RN, programming or speed-up operation. For a given pump,

$$I_{COMP} = (I_{PUMP} / 128) * (FDAC / 5*128) * FRD$$

FRD is the fractional accumulator value.

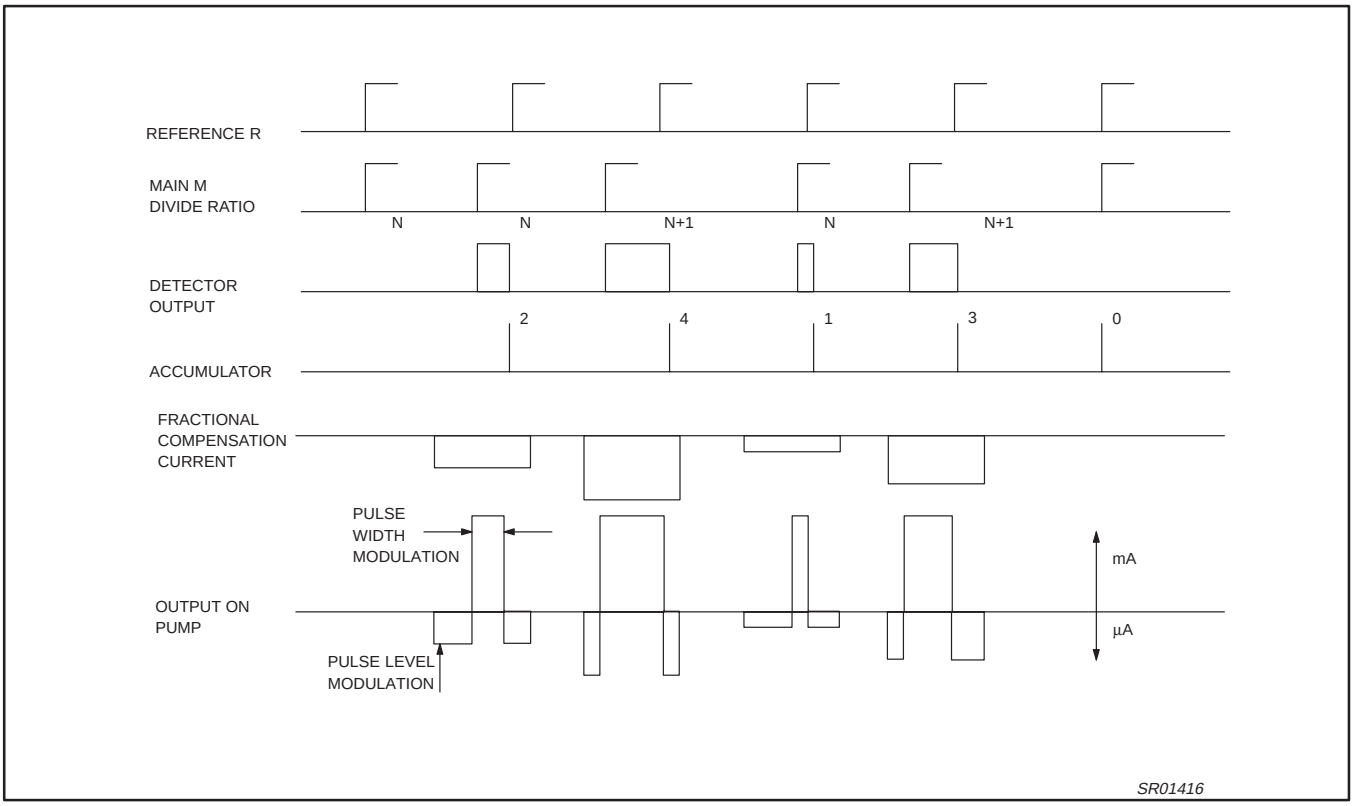


Figure 6. Waveforms for NF = 2, Fraction = 0.4

Fig 6. shows that for a proper fractional compensation, the area of the fractional compensation current pulse must be equal to the area of the charge pump ripple output.

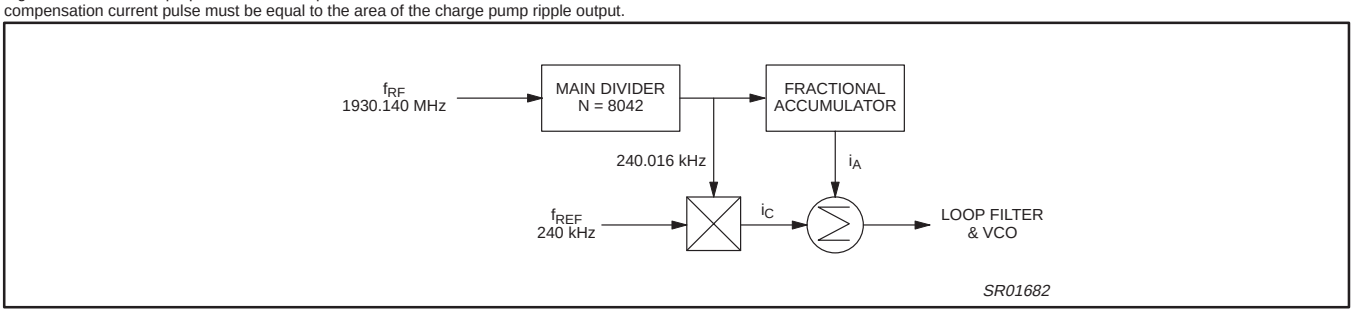


Figure 7. Current Injection Concept

Charge pump currents

CP0	I_{PHP}	I_{PHP-SU}
0	3xIset	15xIset
1	1xIset	5xIset

NOTES
1. $I_{SET}=^{Vset}/_{Rset}$: bias current for charge pumps.
2. I_{PHP_SU} is the total current at pin PHP during speed up condition.

Lock Detect

The output LOCK maintains a logic '1' when the auxiliary phase detector ANDed with the main phase detector indicates a lock condition. The lock condition for the main and auxiliary synthesizers is defined as a phase difference of less than ± 1 period of the frequency at the input $REF_{in+,\ -}$. One counter can fulfill the lock condition when the other counter is powered down. Out of lock (logic '0') is indicated when both counters are powered down.

Power-down mode

The power-down signal can be either hardware (PON) or software (PD). The PON signal is exclusively ORed with the PD bits. If PON = 0, then the part is powered up when PD = 1. PON can be used to invert the polarity of the software bit PD. When the synthesizer is reactivated after the power-down the main and reference dividers are synchronized to avoid possibility of random phase errors on power-up.

Serial programming bus

The serial input is a 3-wire input (CLOCK, STROBE, DATA) to program all counter divide ratios, fractional compensation DAC, selection and enable bits. The programming data is structured into 24 bit words; each word includes 2 address bits. Figure 8 shows the timing diagram of the serial input. When the STROBE goes active HIGH, the clock is disabled and the data in the shift register remains unchanged. Depending on the 2 address bits the data is latched into different working registers or temporary registers. In order to fully program the synthesizer, 3 words must be sent: C, B, and A. Table 1 shows the format and the contents of each word. The D word is for testing purposes only. The data for the fractional compensation DAC, FC is stored by the B word in temporary registers. When the A word is loaded, the data of these temporary registers is loaded together with the main divider ratio.

Serial bus timing characteristics. See Figure 8.

V_{DD} = V_{DDCP} =+3.0V; T_{amb} = +25°C unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	Input rise time	–	10	40	ns
t_f	Input fall time	–	10	40	ns
T_{cy}	Clock period	100	–	–	ns
Enable programming; STROBE					
t_{START}	Delay to rising clock edge	40	–	–	ns
t_W	Minimum inactive pulse width	1/fcomp	–	–	ns
$T_{SU;\overline{E}}$	Enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	Input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	Input data to clock hold time	20	–	–	ns

Application information

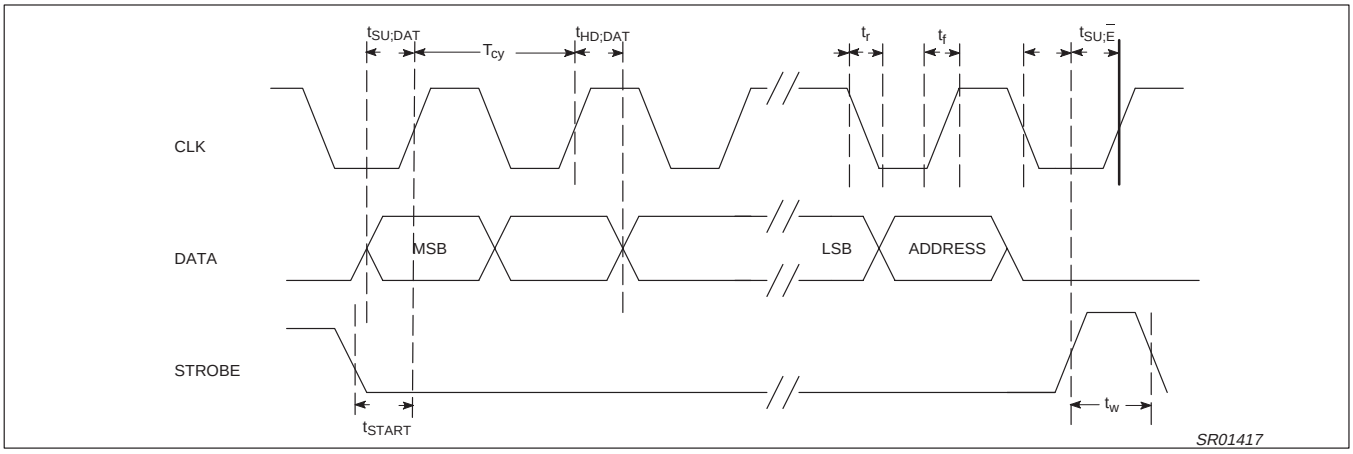


Figure 8. Serial Bus Timing Diagram

Data format

Table 1. Format of programmed data

LAST IN		MSB	SERIAL PROGRAMMING FORMAT				FIRST IN LSB
p23	p22	p21	p20	../..	../..	p1	p0

Table 2. A word, length 24 bits

LAST IN					MSB															LSB	FIRST IN	
Address		fmod	Fractional-N		Main Divider ratio																Spare	
0	0	FM	NF2	NF1	NF0	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	SK1	SK2
Default:		0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0

A word select	Fixed to 00.
Fractional Modulus select	FM 0 = modulo 8, 1 = modulo 5.
Fractional-N Increment	NF2..0 Fractional N Increment values 000 to 111.
N-Divider	N0..N15, Main divider values 512 to 65535 allowed for divider ratio.

Table 3. B word, length 24 bits

ADDRESS		REFERENCE DIVIDER										LOCK		PD		FRACTIONAL COMPENSATION DAC							
0	1	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	L1	L0	Main	Aux	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0
Default:		0	0	0	1	0	1	0	0	0	1	0	0	1	1	0	1	0	1	0	0	0	0

B word select	Fixed to 01
R-Divider	R0..R9, Reference divider values 4 to 1023 allowed for divider ration.
Lock detect output	L1 L0 0 0 Combined main, aux. lock detect signal present at the LOCK pin (push/pull). 0 1 Combined main, aux, lock detect signal present at the LOCK pin (open drain). 1 0 Main lock detect signal present at the LOCK pin. 1 1 Auxiliary loop lock detect signal present at the LOCK pin. When auxiliary loop and main loop are in power down mode, the lock indicator is low.
Power down	Main = 1: power to N-divider, reference divider, main charge pumps, Main = 0 to power down. Aux = 1: power to Aux divider, reference divider, aux charge pump, Aux = 0 to power down.
Fractional Compensation	FC7..0 Fractional Compensation charge pump current DAC, values 0 to 255. Recommended values: FC = 80 for MOD 8; FC = 128 for MOD 5.

Table 4. C word, length 24 bits

Address		Auxiliary Divider													CP		SM			SA		
1	0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	CP1	CP0	SM2	SM1	SM0	SA2	SA1	SA0
Default		0	0	0	0	0	1	1	1	0	0	1	0	1	0	1	1	0	0	0	0	0	0

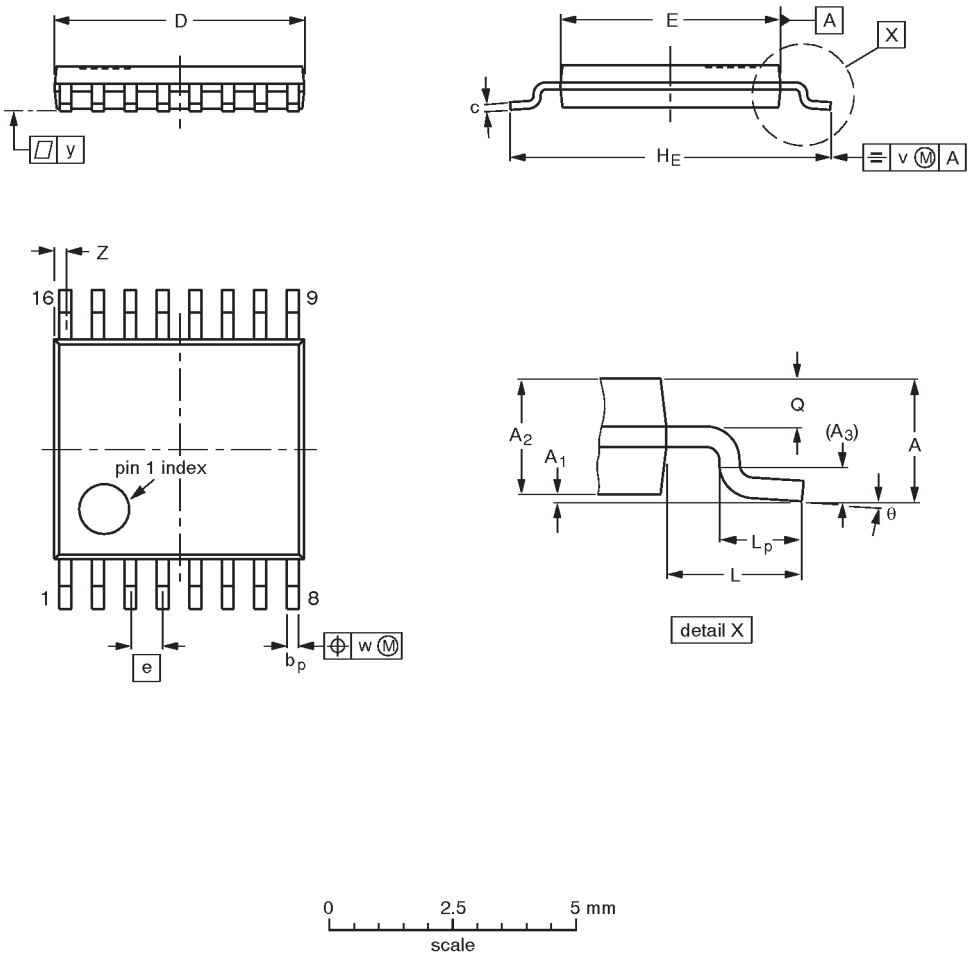
C word select	Fixed to 10
A-Divider	A0..A13, Auxiliary divider values 128 to 16384 allowed for divider ratio.
Charge pump current Ratio	CP1, CP0: Charge pump current ratio, see table of charge pump currents.
Main comparison select	SM comparison divider select for main phase detector.
Aux comparison select	SA Comparison divider select for auxiliary phase detector.

Table 5. D word, length 24 bits

ADDRESS			SYNTHESIZER TEST BITS						SYNTHESIZER TEST BITS														
1	1	0	–	–	–	–	–	Tspu	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
DEFAULT			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Tspu: Speed up	Forces the synthesizer charge pump in speed-up mode all the time. **NOTE**: All test bits must be set to 0 for normal operation.

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~94-07-12~~ 95-04-04

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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